62 included in the writing current circuit 42 via a DRV signal line 108.

The current source 62 is preferably fabricated as part of a complementary metal oxide silicon ("CMOS") IC. As is well known to those skilled in the art of designing CMOS ICs, such ICs include both N-MOS and P-MOS transistors. For the CMOS IC depicted in FIG. 5, the N-MOS transistors are preferably fabricated directly on a silicon semiconductor substrate that contains a p-type dopant material. Alternatively, the P-MOS transistors are formed at wells of semiconductor material which during CMOS IC fabrication are established by placing n-type dopant material into the p-type substrate. Thus, the dopant material used in forming wells for P-MOS transistors in CMOS ICs is complementary to the dopant material of the ICs' substrate. For this type of CMOS IC, the well of n-type semiconductor material established in the p-type substrate for forming P-MOS transistors is frequently referred to as an n-well.

Within each current source 62, a gate of a N-MOS transistor 112 receives the voltage signal VG_IREF present on the current-reference signal line 106. A source and substrate of the N-MOS transistor 112 connect to the VEE power line 104. A drain of the N-MOS transistor 112 connects to a drain of a P-MOS transistor 114. A source and n-well of the P-MOS transistor 114 connect to the VCC power line 102. The drains both of the N-MOS transistor 112 and of the P-MOS transistor 114 connect to a gate of a P-MOS transistor 116. A source of the P-MOS transistor 116 connects both to a gate of the P-MOS transistor 114 and to a drain of a P-MOS transistor 118. A gate of the P-MOS transistor 118 connects to the VEE power line 104 while the source of the P-MOS transistor 118 and the n-wells of both P-MOS transistors 118, 116 connect to the VCC power line 102. A drain of the P-MOS transistor 116 connects to a drain of a N-MOS transistor 122. A gate of the N-MOS transistor 122 connects to the VCC power line 102 while the source and substrate of the N-MOS transistor 122 connect to the VEE power line 104.

Configured in this way with the current-reference voltage signal VG_IREF applied to the gate of the N-MOS transistor 112, the N-MOS transistor 112 operates as a constant current sink for current flowing through the P-MOS transistor 114 from the VCC power line 102. The series connected P-MOS transistor 114 and N-MOS transistor 112 together with the series connected P-MOS transistor 118, P-MOS transistor 116 and N-MOS transistor 122 establish a constant reference voltage V_{REF} at the series connected drains of the N-MOS transistor 112 and P-MOS transistor 114 and the gate of the P-MOS transistor 116. Connection of the source of the P-MOS transistor 116 to the gate of the P-MOS transistor 114 establishes a feedback circuit for controlling and stabilizing the reference voltage V_{REF}.

In addition to being applied to the gate of the P-MOS transistor 116, the constant reference voltage V_{REF} is also applied to a gate of a P-MOS transistor 132. A source of the P-MOS transistor 132 connects to a drain of a P-MOS transistor 134. A gate of the P-MOS transistor 134 connects to the VEE power line 104 while the source of the P-MOS transistor 134 and the n-wells of both P-MOS transistors 134, 132 connect to the VCC power line 102. A drain of the P-MOS transistor 132 connects to a drain of a N-MOS transistor 136. A gate of the N-MOS transistor 136 connects to the DRV signal line 108 while the source and substrate of the N-MOS transistor 136 connect to the VEE power line 104.

Configured in this way, when the on-off digital signal applied to the DRV signal line 108 by one of the bits in the current control register 58 turns the N-MOS transistor 136 on, an electrical current flows through the series connected P-MOS transistors 134, 132 and N-MOS transistor 136. Conversely, when the on-off digital signal applied to the DRV signal line 108 by one of the bits in the current control register 58 turns the N-MOS transistor 136 off, no electrical current flows through the series connected P-MOS transistors 134, 132 and N-MOS transistor 136.

Furthermore, arranged in the configuration described thus far, the P-MOS transistor 118 and the P-MOS transistor 134 are in a current mirror relationship, and the P-MOS transistor 116

During operation of the circuit depicted in FIG. 5, the N-MOS transistor 122 acts to balance the voltages between the drains of the P-MOS transistors 116, 132 so that while the P-MOS transistor 138 is turned off and the N-MOS transistor 136 is turned on the voltage at the gates of P-MOS transistors 114, 142 are identical. Also, while the P-MOS transistor 138 is turned off and the N-MOS transistor 136 is turned on the current-reference voltage signal VG_IREF applied to the gate of the N-MOS transistor 112 controls how much electrical current the current source 62 supplies via the current output line 48 to the laser diode 34.

Furthermore, arranged in the configuration depicted in FIG. 5, the pair of P-MOS transistors 114, 142 are in a current mirror relationship. Thus, the ratio of electrical current flowing through the P-MOS transistors 114, 142 is determined by a size ratio of the P-MOS transistors 114, 142. In this way, the size ratio of the P-MOS transistors 114, 142 determines how much electrical current each of the current sources 62 supplies to the current output line 48 when bits in the current control register 58 turn on the P-MOS transistor 142 included in each of the current sources 62 of the writing current circuit 42.

While each current source 62 may include an output stage of the type depicted in FIG. 5, in the preferred embodiment of the writing current circuit 42 each current source 62 includes an output stage of the type depicted in the circuit diagram of FIG. 6. Those elements depicted in FIG. 6 that are common to the current source 62 illustrated in FIG. 5 carry the same reference numeral distinguished by a prime ("'") designation.

The output stage depicted in FIG. 6 is similar to that depicted in FIG. 5 in receiving an adjustable current-reference signal Voltage Reference Negative ("VREFN") via a negative current-reference signal line 206 which is similar to the current-reference voltage signal VG_IREF depicted in FIG. 5. However, the output stage depicted in FIG. 6 differs from that depicted in FIG. 5 by receiving an adjustable current-reference signal Voltage Reference Positive ("VREFP") via a positive current-reference signal line 208. In the output stage

depicted in FIG. 6, the current-reference signal VREFP is supplied to gates both of the P-MOS transistor 118' and of the P-MOS transistor 134' rather than those gates being connected to the VEE power line 104 as in the output stage depicted in FIG. 5. A complementary voltage reference circuit included in the IC, not illustrated in any of the FIGs., supplies the current-reference signals VREFN and VREFP to each of the current sources 62 included in the writing current circuit 42. Similar to the output stage depicted in FIG. 5, data supplied by the control processor 14 to the complementary voltage reference circuit controls the voltages of the VREFN and VREFP signals.

The output stage depicted in FIG. 6 further differs from that depicted in FIG. 5 by including a first resistor 212 connected between the source of the N-MOS transistor 112' and the VEE power line 104'. Also, a second resistor 214 connects between the n-well of the P-MOS transistor 142' and the VCC power line 102'. Lastly, the output stage depicted in FIG. 6 differs from that depicted in FIG. 5 by including a third resistor 222 and a capacitor 224 that connect in series between the VCC power line 102' and the junction of the drains respectively of the N-MOS transistor 112' and P-MOS transistor 114' and the gates respectively of the P-MOS transistor 116' and P-MOS transistor 132'. The resistors 212, 214 and 222 are approximately 100 ohms, and the capacitor 224 is approximately 5 pico-farads.

Adding the current-reference signal VREFP for controlling operation of the P-MOS transistor 118' and the P-MOS transistor 134' permits adjusting the charging current supplied to the current output line 48 by the P-MOS transistor 142' by varying the voltage VREFP. In this way it becomes possible for the writing current circuit 42 to provide the same rise time and same overshoot for electrical current supplied to the laser diode 34 when the P-MOS transistor 138 initially turns off and the N-MOS transistor 136 initially turns on regardless of power level supplied by the current source 62. Addition of the resistor 212 improves the linearity of the current mirror relationship between the P-MOS transistor 114' and the P-MOS

transistor 142' across a wider power level range. The resistor 214 in combination with the inherent source to n-well parasitic capacitance of the P-MOS transistor 142 form an embedded low pass filter at the output of the current source 62. The presence of this embedded low pass filter at the output of the current source 62 tends to reduce overshoot and undershoot in the current which the P-MOS transistor 142 supplies to the current output line 48. Lastly, addition of the series connected resistor 222 and capacitor 224 reduces the possibility that the feedback circuit formed by the P-MOS transistor 114' and the P-MOS transistor 116' may oscillate during high speed switching.

Industrial Applicability

Depending upon specific recording conditions, the electrical current which the writing current circuit 42 in accordance with the present invention supplies to the laser diode 34 when recording onto a DVD at 16X increases from a nominal value of approximately ten milliamperes ("ma") at time t_0 in FIG. 2 to several hundred ma at time t_1, a time interval of approximately one-half (0.5) nanosecond. When recording onto a DVD at 16X, the maximum electrical current supplied to the laser diode 34, I_p, may be as great as 500 ma.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is purely illustrative and is not to be interpreted as limiting. For example, a writing current circuit 42 in accordance with the present invention may include more or fewer than six (6) thermometer code registers 52. Similarly, a writing current circuit 42 in accordance with the present invention may include more or fewer than sixty-four (64) current sources 62. While the current source 62 preferably employs a P-MOS transistor 142 for supplying electrical current to the laser diode 34 via the current output line 48, a current source 62 in accordance with the present invention may instead use a N-MOS transistor therefor. Consequently, without departing from the spirit and scope of the invention, various alterations, modifications, and/or alternative applica-